CBCS SCHEME

USN | | | | | | | | | | |

15NT34

Third Semester B.E. Degree Examination, Jan./Feb. 2021

MOSFETS and Digital Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain with neat diagrams the construction of JFET. Mention its characteristics. **(08 Marks)**

b. With the help of neat diagrams, explain n-well MOS transistor fabrication process. **(08 Marks)**

OR

2 a. Write a short note on channel length modulation and subthreshold conduction. **(05 Marks)**

b. Explain the VI characteristics of MOSFET. **(05 Marks)**

c. Explain the SOI process with its merits and demerits. **(06 Marks)**

Module-2

3 a. Explain the CMOS inverters along with power dissipation equations. **(10 Marks)**

b. Give the scaling factors for gate area, gate delay and saturation current. **(06 Marks)**

OR

4 a. Explain with neat diagram the realization of two input NOR and NAND gate using CMOS technology. **(10 Marks)**

b. Explain the AOI and OAI gate with example. **(06 Marks)**

Module-3

5 a. Discuss the working principle of CMOS positive edge triggered latch with neat diagram. **(10 Marks)**

b. Distinguish between latch and registers. **(06 Marks)**

OR

6 a. With neat diagram explain the operation of JK flip flop. **(08 Marks)**

b. Explain mux based latch. **(04 Marks)**

c. Define setup time and hold time. **(04 Marks)**

Module-4

7 a. Define registers. Explain SISO, SIPO and PISO shift registers. **(10 Marks)**

b. Design a Mod – 5 synchronous up counter using T flip flop. **(06 Marks)**

OR

8 a. Write a note on Ring and Johnson counter. **(06 Marks)**

b. Design a synchronous counter using JK flip flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 - - - - - . **(10 Marks)**

Module-5

9 a. Draw the Melay and Moore synchronous machine models. Label the excitation variables, state the variables, input and output variable in both the diagrams. **(06 Marks)**

b. Design a Mod 6 synchronous counter using JK flip flop to count the numbers. **(10 Marks)**

OR

10 a. Give output function excitation table and state transition diagram by analyzing the sequential circuit shown in Fig Q10 (a). **(08 Marks)**

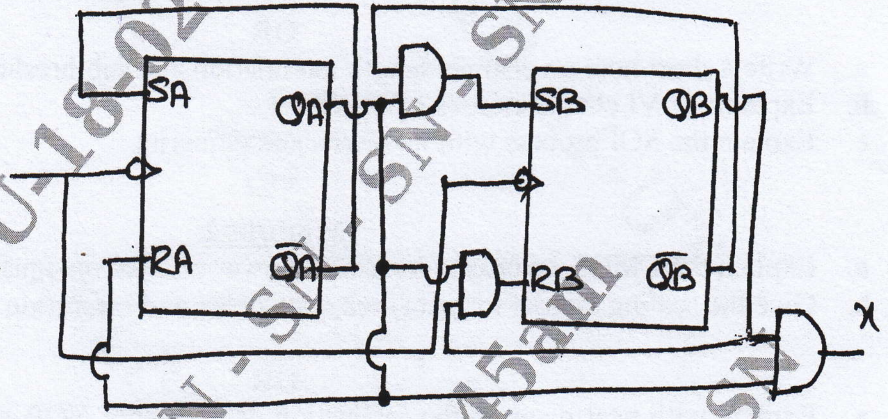

Fig Q10(a)

b. Design a sequence detector to detect sequence 1101. **(08 Marks)**

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